REMARKS

Reconsideration is respectfully requested. Claims 1-19 are present in the application. Claims 5-7, 10 and 11 are amended herein. New claims 20-27 are presented.

Claims 1-19 are rejected under 35 U.S.C. §112, first paragraph, as allegedly not enabled by the specification. Applicant respectfully traverses.

The Examiner says that applicant admits in the specification that there is a 2 cycle delay in a read operation and that therefore the transfer to at least two destinations substantially simultaneously is not enabled. Applicant disagrees. The timing chart and portion of the specification in question merely shows the timing of signals to set the DSP chip into a read operation. The RX_Data 34 appears on the bus for reading by the DSP and writing to the memory storage only at the timing shown. That is, at cycle 9, for example, data W3 is present on the bus. That is the only time that the transfer from the bus to both the DSP and the memory device can be effected for a specific data unit (W3, in the example discussed herein). The data cannot start being read by the DSP from the bus before it appears on the bus. Similarly, the data cannot be read after it is no longer on the bus. Applicant respectfully submits that the specification is enabling for what is claimed. The data is present for a set period of time (typically one

clock cycle, but in the case of W1, it is 2 clock cycles in the particular embodiment illustrated) and during that time transfer to the first data source as a read and to the second data source as a write are effected. Merely because the timing of operation of one device in the illustrated example requires a read signal to be enabled before the read data is present does not make the specification non-enabling. It only shows the timing required for supplying signals to the various devices to get them to behave in the manner applicant desires in this embodiment. Further, the specification at page 4, lines 23-24, referred to by the Examiner, is merely stating that in the particular timing required, first, row address data is supplied to the memory device, then, 2 clock cycles later, a READ signal is supplied on the DSP device command signal line and the column selection signal COL is supplied to the memory device. This does not state that a 2 cycle latency is present between a read and a write. It merely teaches the timing of the control signals to effect the various devices to properly access the data in the RX_Data bus during the short time that each data W1, W2, W3, etc., is present.

Applicant respectfully requests that the 35 U.S.C. §112, first paragraph rejection be withdrawn.

Claims 10 and 11 are rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. Applicant thanks the Examiner for providing suggested wording to address the Examiner's concern. While it is believed that the claims were clear as presented originally, to further prosecution, these claims have been amended to recite "said FIFO data source".

Claims 1, 4-8, 12, 14-16 and 19 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Masterson et al (U.S. 5,073,851). Applicant respectfully traverses.

From study of the rejection, applicant respectfully submits that the Examiner is rejecting something that is not claimed. The claimed invention relates to data being presented on a bus, and that data is, at substantially the same time, read into one device as a read operation and written to another device as a write operation.

Masterson is doing something different and one would not be motivated to combine Masterson with AAPA, and even if such combination were made, applicant's invention would not result.

Masterson is concerned with transferring data between memory and cache. If memory were considered DEV#1 (abbreviation for device #1) and cache were considered DEV#2 (abbreviation for device #2), then the operation taught by Masterson is as follows for transfer of N data units:

At Time T1, Read 1st data from DEV#1, no operation in DEV#2

At T2, Read 2nd data from DEV#1, write 1st data to DEV#2

At T3, Read 3rd data from DEV#1, write 2nd data to DEV#2

. . .

At Time N, Read Nth data from DEV#1, write N-1st data to DEV#2

At Time N+1, no read operation, write Nth data to DEV#2.

This is not related to what applicant claims.

Discussing the operation of applicant's methods and devices in a similar format to the above discussion of Masterson's operation, applicant's operations would be as follows:

Assuming DEVA is device A, a first device, and DEVB is device B, a second device, to transfer N data units:

At Time T1, DEVA reads first data, DEVB writes first data

At Time T2, DEVA reads second data, DEVB writes second data

At Time T3, DEVA reads third data, DEVB writes third data

. . .

At Time N, DEVA reads Nth data, DEVB writes Nth data.

The above illustrates a difference. Masterson specifically teaches away from applicant's claimed invention. Even if Masterson were related to applicant's invention (which it is not), to transfer N units of data requires N+1 operation cycles in Masterson.

Claim 1 discusses, removing some of the details in order to illustrate applicant's point, transferring **a unit** of data, which includes supplying **said unit** of data to a first destination and supplying **said unit** of data to a second destination. In making

the rejection, the Examiner has instead converted this to be transferring a **first data** to device #1 and transferring a **second data** to device #2. But that is not what applicant claims.

The Examiner indicates that it is assumed that the "a unit of data" for a read operation is different from the subject matter "unit of data" for a write operation. So, what the Examiner is rejecting is not even what is recited in the claims. Instead, the Examiner is changing the interpretation of what the claims say into something different that what they say. Note the emphasized portions above. A purpose of applicant's invention is to speed operations, to avoid having to transfer data across a bus twice. Thus an advantage is provided as a unit of data is substantially simultaneously written to one device while another device is reading the unit of data. That is the same unit of data. The timing chart of FIG 2 shows item 34, that the data appears on the bus once. It is not repeated. This speeds operation.

A corresponding argument applies to claim 8, wherein the selected ones of discrete units of data are written to the memory and read to the microprocessor substantially simultaneously. Claim 8 is also therefore allowable.

The respective dependent claims are also submitted to be allowable.

Claims 2, 3, 9-11 and 13 rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of Masterson and

further in view of DeSouza et al, U.S. 5,379,289. Applicant respectfully traverses.

DeSouza adds nothing that would overcome the conceptual difference between Masterson and applicant's methods and devices as noted above. Even if there were motivation to combine these documents' teachings, the resulting device and methods would still carry the above-noted difference wherein while first data is read, no data is written, and when second data is read, the first data is written, etc., requiring N+1 steps for N data. This explicitly teaches away from applicant's simultaneous read/write concept. Therefore, claims 2, 3, 9-11 and 13 are submitted to be allowable.

Claims 17 and 18 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of Masterson and further in view of IBM Technical Disclosure Bulletin, December 1979, Circuit for Tracing Branch Instructions. Applicant respectfully traverses.

The IBM bulletin relates to a system for providing an audit trail of branch instructions. So, an instruction address register is recorded, but an address pointer is not incremented until a branch instruction occurs. Thus, only the points where branch instruction addresses occur are recorded. The purpose is to not fill the trace memory to its capacity, by only recording branch instruction addresses, rather than all addresses. It is respectfully submitted that one would not look to circuits for

avoiding filling trace memory when tracing branch instructions in a processor under test when constructing methods and devices such as applicant's, wherein the goal is to speed operations rather than to save memory capacity.

However, even if one were motivated to look to the IBM bulletin, the lack of teaching by Masterson as discussed above is not changed by the addition of the IBM bulletin. Accordingly claims 17 and 18 are submitted to be allowable.

New claims 20-27 are added herein. The claims relate to methods for transferring a unit of data on a bus from a source to at least two separate destination devices with a single bus transfer from the source. Support for these claims is found in the specification as filed at, for example, page 6, lines 7-9. New claims 20-27 are submitted to be allowable.

In light of the above noted amendments and remarks, this application is believed in condition for allowance and notice thereof is respectfully solicited. The Examiner is asked to contact applicant's attorney at 503-224-0115 if there are any questions.

Respectfully submitted,

James H. Walters, Reg. No. 35,731

Customer number 802
DELLETT AND WALTERS
Suite 1101
310 S.W. Fourth Avenue
Portland, Oregon 97204 US
(503) 224-0115
DOCKET: F-316

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